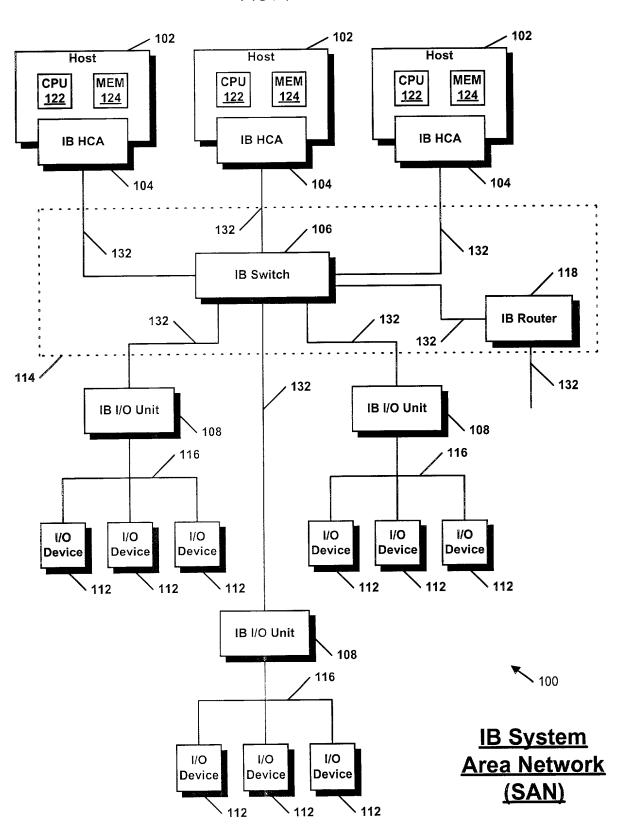
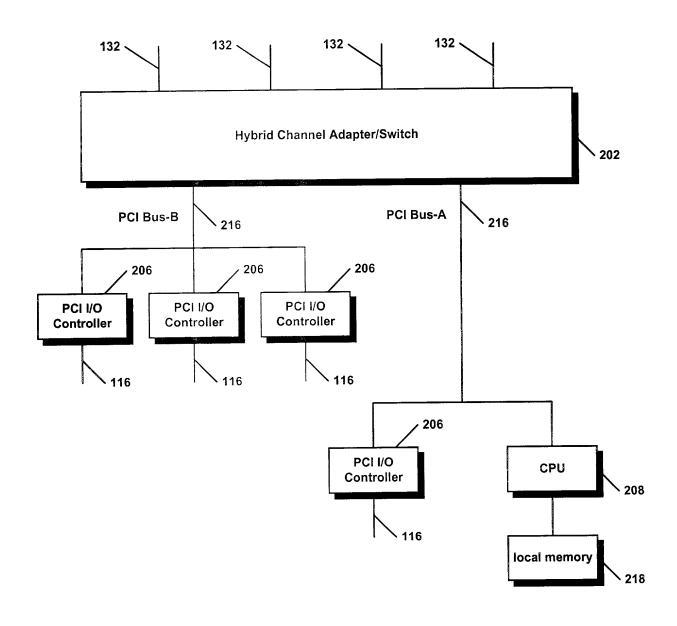
FIG. 1

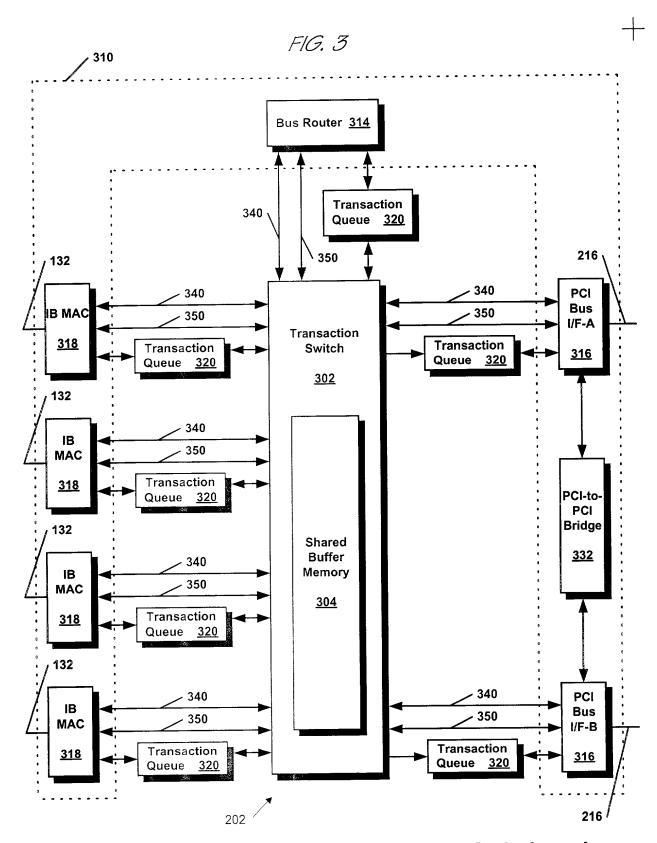




IB Hybrid Channel Adapter/Switch

+

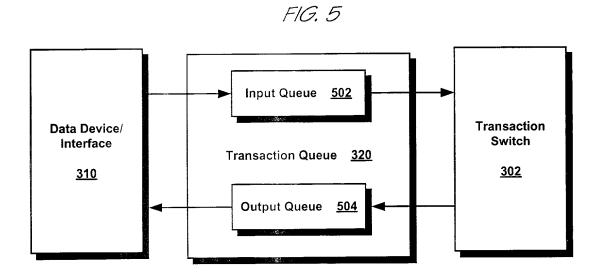
+



IB Hybrid CA/Switch with Transaction Switch and Shared Buffer Memory

FIG. 4 340 340 20 IB MAC IB MAC Mux <u>318</u> 402 <u>318</u> Mux SRAM <u>404</u> <u>406</u> 340 340 20 IB MAC IB MAC Mux <u>318</u> <u>402</u> <u>318</u> 340 SRAM Mux 340 20 <u>406</u> <u>404</u> IB MAC **B MAC** Mux <u>318</u> <u>402</u> <u>318</u> 340 340 20 B MAC SRAM Mux IB MAC Mux <u>318</u> <u>404</u> <u>406</u> <u>318</u> <u>402</u> 340 340 20 PCI I/F PCI I/F Mux 8 <u>316</u> <u>316</u> <u>402</u> SRAM Mux <u>406</u> <u>404</u> 340 340 20 PCI I/F PCI I/F Mux <u>316</u> <u>402</u> <u>316</u> 340 340 20 Mux<u>402</u> 304 340 \ 20 Bus Bus Mux Router Router <u>402</u> <u>314</u> <u>314</u> SRAM Mux 20 406 <u>404</u> Mux 402 \ 340 340 350 Control Logic 408 Port Switch Mapping Buffer Manager 414 **Transaction** Table <u>412</u> Queues 302 <u>320</u>

**Transaction Switch Data Paths** 



### Transaction Queues

FIG. 6

1 Er	me LNH	Destination QP	Packet Length	VL	Buffer Address
1	606	608	612	<u>614</u>	616

#### **MAC Input Queue Entry**

600

FIG. 7

Tag	PCI Address/Port	Length	Offset	VL	Туре	Buffer Address
<u>702</u>	<u>704</u>	<u>706</u>	<u>708</u>	<u>712</u>	<u>714</u>	<u>716</u>

FIG. 8

Not Raw 802	Tag 804	Packet Length <u>806</u>	VL 808	Buffer Address <u>812</u>
	(4857) (1953)			

# MAC Output Queue Entry

800

FIG. 9

902 904 906 908 912 914 916	Port	Frame Error	LNH	Destination QP	Length	VL	Buffer Address
	902		<u>906</u>	, <u>908</u>	<u>912</u>	<u>914</u>	

### **Bus Router Output Queue Entry**

**\** 900

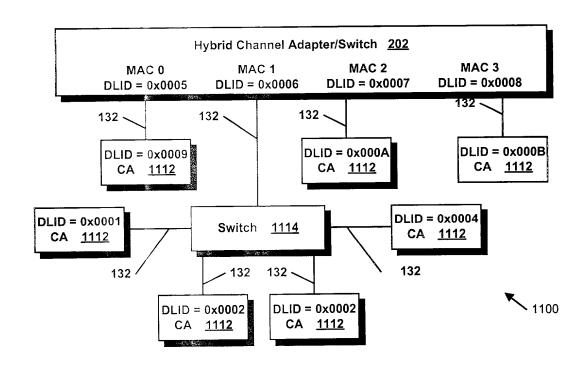
FIG. 10

Tag	PCI Address	Length	Offset	PCI Type	Buffer Address
1002	<u>1004</u>	<u>1006</u>	<u>1008</u>	<u>1012</u>	<u>1014</u>

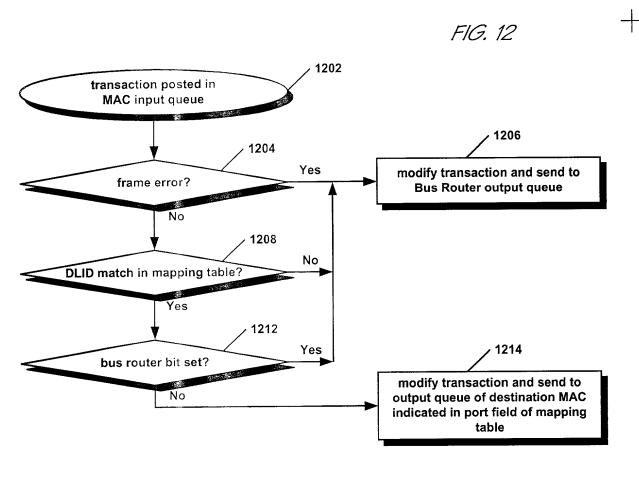
## PCI Output Queue Entry

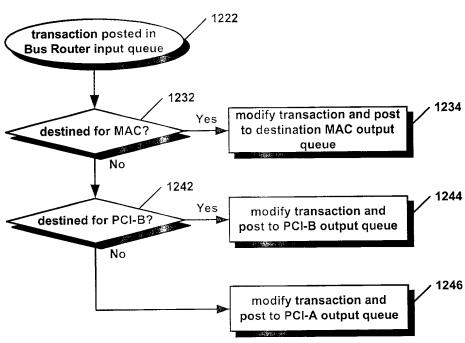
1000

				!
1 5 5 2	Bus Router 1102	Port <u>1104</u>	DLID <u>1106</u>	Valid <u>1108</u>
0	1	0	0x0005	1
1	1	1	0x0006	1
2	1	2	0x0007	1
3	1	3	0x0008	1
4	0	1	0x0001	1
5	0	1	0x0002	1
6	0	1	0x0003	1
7	0	1	0x0004	1
8	0	0	0x0009	11
9	0	2	0x000A	1
10	0	3	0x000B	1
11	0	2	-	0
12	0	1	•	0
13	0	3	-	0
14	0	2	•	0
15	0	2	0x0007	1
	1 2 3 4 5 6 7 8 9 10 11 12 13	1102   0 1   1 1   2 1   3 1   4 0   5 0   6 0   7 0   8 0   9 0   10 0   11 0   12 0   13 0   14 0	1102 1104   0 1 0   1 1 1   2 1 2   3 1 3   4 0 1   5 0 1   6 0 1   7 0 1   8 0 0   9 0 2   10 0 3   11 0 2   12 0 1   13 0 3   14 0 2	Bus Router 1102     Port 1104     DLID 1106       0     1     0     0x0005       1     1     1     0x0006       2     1     2     0x0007       3     1     3     0x0008       4     0     1     0x0001       5     0     1     0x0002       6     0     1     0x0003       7     0     1     0x0004       8     0     0     0x0009       9     0     2     0x000A       10     0     3     0x000B       11     0     2     -       12     0     1     -       13     0     3     -       14     0     2     -

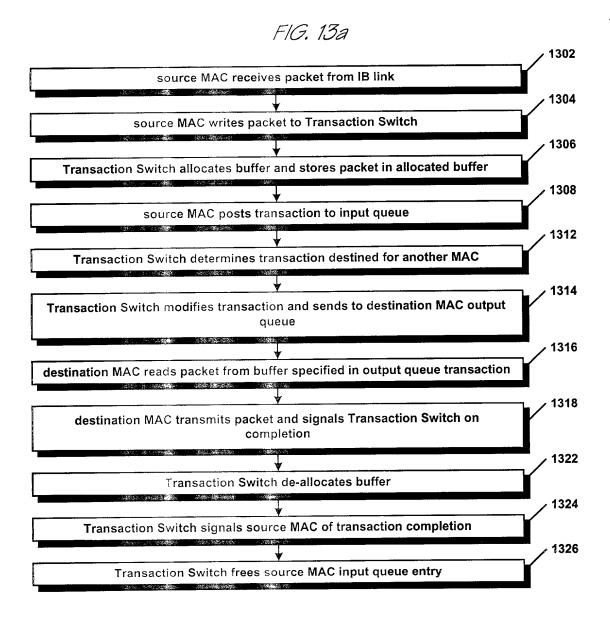


Port Switch Mapping Table in Example Network



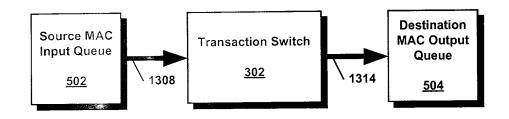


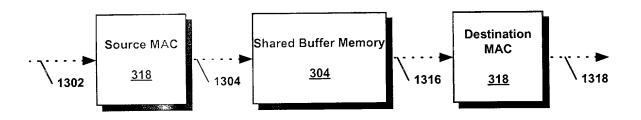
**Transaction Switching** 

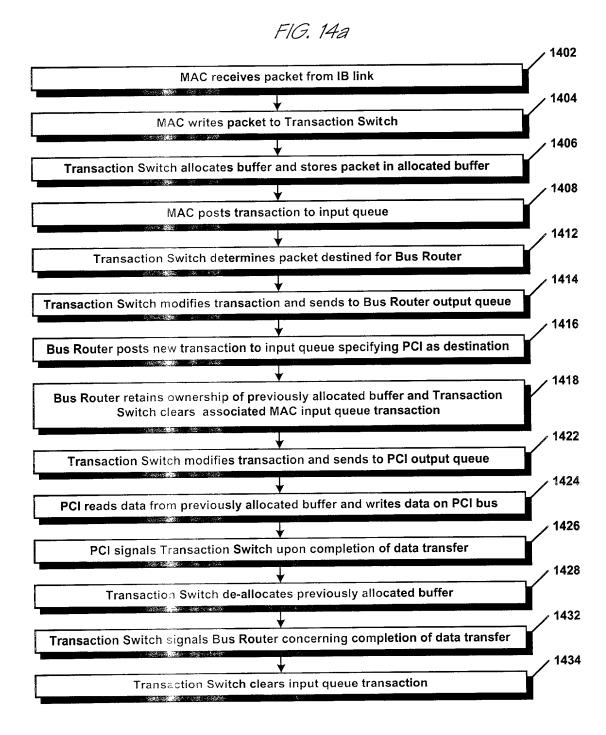


### Packet Switching Operation



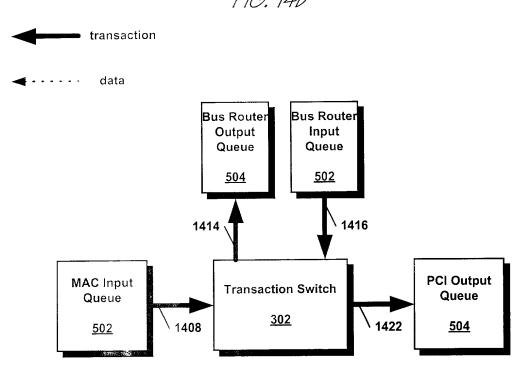


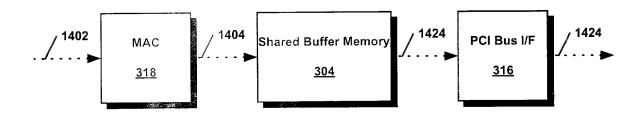


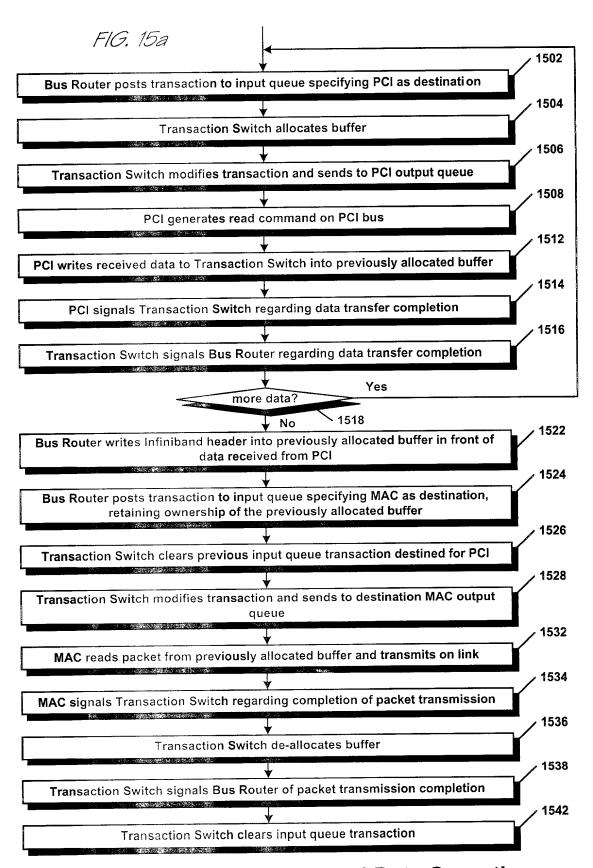


#### Packetized Data to Addressed Data Operation

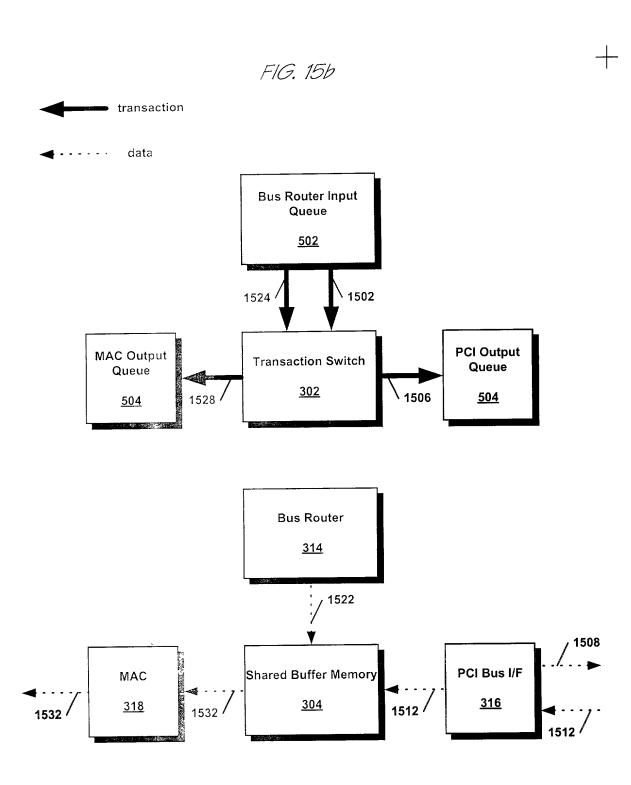
FIG. 14b

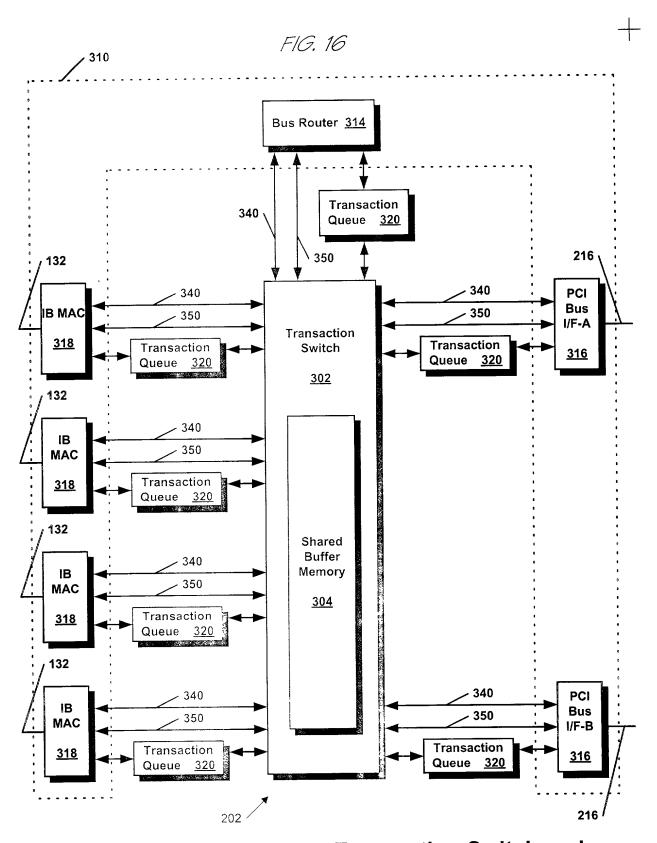






**Addressed Data to Packetized Data Operation** 





IB Hybrid CA/Switch with Transaction Switch and Shared Buffer Memory

FIG. 17

PCI Address	Length		PCI Cycle Type
<u>1702</u>	<u>1704</u>	Address <u>1706</u>	1708

# PCI Input Queue Entry

1700

